Claims

We Claim:

1. A high frequency integrated circuit structure comprising:

a body of semiconductor material having a plurality of isolated active regions;

internal circuitry formed in a first active region;

a first silicon controlled rectifier device formed in a second active region, the first silicon controlled rectifier device comprising a first doped region of a first conductivity type, a first well region of the first conductivity type, a buried layer of a second conductivity type, a second well region of the first conductivity type, and a second doped region of the second conductivity type; and

a second silicon controlled rectifier device comprising a third doped region of the first conductivity type, the second well region, the buried layer, the first well region, and a fourth doped region of the second conductivity type, wherein the first and second silicon controlled rectifier devices are coupled to the internal circuitry and form an ESD structure for protecting the internal circuitry against positive and negative ESD stresses.

2. The high frequency integrated circuit structure of claim 1 wherein the body of semiconductor material comprises:

a semiconductor wafer having the first conductivity type;

a first semiconductor layer formed over the semiconductor wafer, wherein the first semiconductor layer comprises the first conductivity type, wherein the first semiconductor layer has a lower dopant concentration than the semiconductor wafer, and wherein the buried layer is formed over the first semiconductor layer; and

a second semiconductor layer formed over the buried layer, wherein the second semiconductor layer comprises the second conductivity type and has a lower dopant concentration than the buried layer, and wherein the first and second wells are formed in the second semiconductor layer, and wherein the first and fourth doped regions are in the first well, and wherein second and third doped regions are in the second well.

3. The high frequency integrated circuit device of claim 2 further comprising:

a first ohmic contact coupling the first and fourth doped regions; and

a second ohmic contact coupling the second and third doped regions.

4. The high frequency integrated circuit device of claim 2 further comprising a deep contact trench extending from a surface of the second semiconductor layer into the semiconductor wafer.

5. The high frequency integrated circuit device of claim 2 further comprising a field dielectric region formed on a surface of the second semiconductor layer between the first and second wells.

6. The high frequency integrated circuit structure of claim 2, wherein the first semiconductor layer has a dopant concentration of approximately $1.0x10^{13}$ atoms/cm^3

7. the high frequency integrated circuit structure of claim 2, wherein the first semiconductor layer has a thickness from about 1.5 microns to about 3.0 microns.

8 The high frequency integrated circuit structure of claim 1 further comprising a deep isolation trench formed in the semiconductor substrate for isolating the ESD structure from the internal circuitry.

9. A symmetrical SCR device comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type formed over the first semiconductor layer, wherein the second semiconductor layer has a lower dopant concentration than the first semiconductor layer;

first and second wells comprising a second conductivity type formed in the second semiconductor layer, wherein the first and second wells are spaced apart;

first and second doped regions formed in the first well, wherein the first doped region comprises the first conductivity type and the second doped region comprises the second conductivity type, and wherein the first and second doped regions are electrically coupled; and

third and fourth doped regions formed in the second well, wherein the third doped region comprises the first conductivity type and the fourth doped region comprises the second conductivity type, and wherein the third and fourth doped regions are electrically coupled.

10. The SCR device of claim 9 further comprising:

a semiconductor substrate of the second conductivity type;

a fourth semiconductor layer of the second conductivity type formed over the semiconductor substrate, wherein the first semiconductor layer is formed over the fourth semiconductor layer, and wherein the fourth semiconductor layer has a lower dopant concentration than the semiconductor substrate.

11. The SCR device of claim 10 wherein the fourth semiconductor layer has a dopant concentration of about $1.0x10^{13}$ atoms/cm^3, and a thickness of about 1.5 to about 3.0 microns

12. The SCR device of claim 10 further comprising a deep isolation trench extending from a surface of the second semiconductor layer into the semiconductor substrate.

13. The SCR device of claim 10 further comprising a deep contact trench extending from a surface of the third semiconductor layer into the first semiconductor layer.

14. The SCR device of claim 9 further comprising an isolation region formed on a surface of the second semiconductor region between the first and second wells.

15. The SCR device of claim 9 wherein the first conductivity type comprises n-type, and wherein the second conductivity type comprises p-type.

16. A method for forming a high frequency SCR device including the steps of:

providing a semiconductor substrate including a first semiconductor layer of a first conductivity type, a second semiconductor layer of a second conductivity type over the first semiconductor layer, and a third semiconductor layer over the second semiconductor layer, wherein the third semiconductor layer comprises the second conductivity type, and wherein the third semiconductor layer has a lower dopant concentration than the second semiconductor layer;

forming first and second wells in the third semiconductor layer, wherein the first and second wells comprise the first conductivity type, and wherein the first and second wells are spaced apart;

forming first and second doped regions in the first well, wherein the first doped region comprises the first conductivity type, and the second doped region comprises the second conductivity type; and

forming third and fourth doped regions in the second well, wherein the third doped region comprises the first conductivity type, and wherein the fourth doped region comprises the second conductivity type.

17. The method of claim 16 wherein the step of providing the semiconductor substrate includes providing a semiconductor substrate having a fourth semiconductor layer formed between the first semiconductor layer and the second semiconductor layer, wherein the fourth semiconductor layer comprises the first conductivity type, and wherein the fourth semiconductor layer has a lower dopant concentration than the first semiconductor layer.

18. The method of claim 16 further comprising the steps of:

forming an isolation region on a surface of the third semiconductor region between the first and second wells;

forming a first ohmic contact coupling the first and second doped regions; and

forming a second ohmic contact coupling the third and fourth doped regions.

19. The method of claim 16 further comprising the step of forming a deep isolation trench that surrounds the high frequency SCR device, and that extends from a surface of the third semiconductor layer into the first semiconductor layer.

20. The method of claim 16 further comprising the step of forming a deep contact trench extending from a surface of the third semiconductor layer into the first semiconductor layer.